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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,466	11/24/2003	Anthony Correale JR.	YOR920030373US1	4073

33233 7590 08/31/2005

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EXAMINER	
CHANG, DANIEL D	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 08/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,466	CORREALE ET AL.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Specification

The disclosure is objected to because of the following informalities: on page 9, lines 13 and 16, serial numbers need to be filled out. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 7-10, 12-15, 17-23, 25-28, and 30 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Feller (EP 125,733 A1).

Feller clearly discloses a first buffer/inverter (10; see page 7, lines 16+), a second buffer/inverter (20), and a supply select/threshold drop element (30).

Regarding claim 17, the recitation, "the FET is a high threshold voltage FET" does not mean much because it can be interpreted that any FET has a high threshold voltage compared to any other FET having lower threshold voltage.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6, 11, 16, 24, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Feller.

Regarding claims 6, 16, and 24, Feller clearly discloses all the features of the claimed invention but does not disclose that the at least one diode connected NFET is a plurality or a pair of series connected NFET diodes.

However, it is well known in the art that when more voltage drop is desired, more diodes are connected in series. Therefore, it would have been obvious at the time the invention was made to an ordinary skilled in the art to have provided NFET diode (N4) of Feller with more NFET diode(s) in series in order to provide more voltage drops.

Regarding claims 11 and 29, Feller clearly discloses all the features of the claimed invention but does not disclose that the CMOS inverter includes an NFET having a threshold higher than other NFETs in the level converter.

However, it is well known in the art that the NFET of a CMOS inverter having high threshold voltage reduces leakage current. Therefore, it would have been obvious at the time the invention was made to an ordinary skilled in the art to have provided NFET of Feller with higher threshold voltage in order to reduce leakage current.

Response to Arguments

Applicant's arguments filed June 21, 2005 have been fully considered but they are not persuasive.

Regarding claims 1 and 12, applicant argues on page 10 of the Amendment filed 6/21/05, that "Claims 1 and 12 are amended to recite that 'standby power is substantially eliminated' in

the level converter when the input/output is high. This is not taught nor suggested by Feller." However, TTL circuit not only receives 2.0 volts but also receives voltage up to 5.0 volts. Therefore, assuming 3.0V is an input voltage, Vsg=3.6V - 3.0V = 0.6V which is less than 1.4V. (see page 10, first paragraph for applicant's argument). So current does not flow and standby power is substantially eliminated.

Regarding claim 19, applicant argues on page 10 of the Amendment filed 6/21/05, that "Claim 19 is drawn to an IC with high and low voltage circuits in the IC being interfaced by such a level converter, which Feeler neither discloses nor suggests." However, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Morris (US 5,304,867) discloses TTL-to-CMOS input buffer with high speed and low power.

Foss (US 4,786,830) discloses CMOS input buffer circuit for TTL signals.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

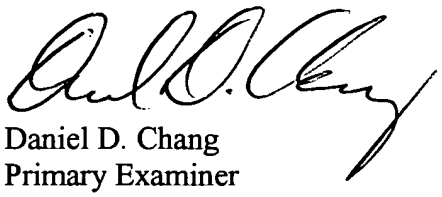
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Daniel D. Chang
Primary Examiner
Art Unit 2819

dc

DANIEL CHANG
PRIMARY EXAMINER